MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information		
معلومات المادة الدراسية		

Module Title	Digital Logic	Module Delivery
Module Type	Basic	☒ Theory
Module Code	IT102	☐ Lecture
ECTS Credits	6	☒ Lab
		☐ Tutorial
SWL (hr/sem)	150	☒ Practical
		☐ Seminar

Module Level	1	Semester of Delivery	1
Administering Department	Information Technology	College	College of Science
Module Leader	Nabeel Sadiq Abdel Abbas	e-mail	nabeel@uowa.edu.iq
Module Leader's Acad. Title	Assistant	Module Leader's Qualification	Mcs
Module Tutor	-	e-mail	-
Peer Reviewer Name	-	e-mail	-
Scientific Committee Approval Date	-	Version Number	0.1

Relation with other Modules		
العلاقة مع المواد الدراسية الأخرى		

Prerequisite module		Semester	
Co-requisites module		Semester	

Module Aims, Learning Outcomes and Indicative Contents
أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية
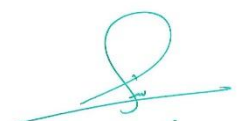
Module Objectives أهداف المادة الدراسية	1. Provide students with basic information about digital logic and logic circuits. 2. Increasing students' horizons in the fields of computer science and digital development. 3. Developing the students' English language by teaching the subject in English. 4. Providing students with applied and experimental skills through practical subjects and laboratories. 5. Familiarize students with the latest developments in the fields of different sciences and the technology emanating from them. 6. Developing the student's ability to research and providing him with scientific research contexts. 7. Develop students' ability to analyze and link information and conclusion. 8. Enhancing the scientific spirit in the interpretation of phenomena, discussion, and dialogue. 9. Consolidation of conviction in the integration of sciences and their universality towards the truth. 10. Working on refining the student's personality and discovering his inclinations and talents through scientific and cultural activities. 11. Enhancing the spirit of teamwork through the participation of students in laboratory work or the completion of joint scientific research. Establish values and ideals Higher among them is respect for instructions, discipline, respect for the institution to which the student belongs, and preservation of its property.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Knowing the numerical number systems used in logical circuits and performing arithmetic operations on them. 2. Knowledge of logical circuits and their design methods. 3. Simplify logic circuits by simplifying their equations. 4. Full knowledge of digital meters, dividers, and other electronic circuits. 5. Full knowledge of the use of signs and their representation in binary numbers. 6. Full knowledge of how to convert between number systems used in numerical operations. 7. How to integrate digital portals together and methods of calculating their outputs. 8. Design counters and dividers and link them together
Indicative Contents المحتويات الإرشادية	1. Introduction to Digital Logic and Logic Circuits • Overview of digital logic and its significance in computer science and digital development • Introduction to logic circuits and their role in processing digital information 2. Logic Gates and Circuit Design • Exploration of fundamental logic gates (AND, OR, NOT, XOR, NAND, NOR) • Designing and analyzing logic circuits using gates • Application of De Morgan's theorem for circuit simplification 3. Combinational Logic Circuits • Understanding the design and operation of combinational logic circuits • Implementation of multiplexers, demultiplexers, encoders, and decoders

• Building adders, subtractors, and comparators
4. Sequential Logic Circuits
• Introduction to sequential logic circuits and their behavior
• Study of flip-flops and latches for storing and transferring data
• Analysis and design of synchronous and asynchronous sequential circuits
5. Digital Integrated Circuits
• Types and characteristics of digital integrated circuits (TTL, CMOS, FPGA)
• Understanding IC packaging, pin configurations, and datasheets
• Testing, troubleshooting, and selecting appropriate ICs for specific applications.
6. Practical Applications and Research Focus
• Hands-on experiments in laboratory settings to apply learned concepts.
• Exploring emerging trends and advancements in digital logic and circuits
• Developing research skills and methodologies for investigating digital systems

Learning and Teaching Strategies
استراتيجيات التعلم والتعليم

Strategies	• Giving lectures • Performing software tasks in laboratories • Scientific discussions and dialogues and asking questions. • The completion of tasks by student work teams in the laboratory

Student Workload (SWL)
الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	65	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	85	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعيا	6
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5 and 10	
	Assignments	2	10% (10)	2 and 12	
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	
	Final Exam	3hr	50% (50)	16	
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Numbers system
Week 2	Binary, BCD, octal, Hex Numbers
Week 3	Converting Binary Arithmetic
Week 4	1's and 2's Complements of Binary Numbers Signed Numbers
Week 5	Logic Gate
Week 6	Boolean Algebra and Logic Simplification
Week 7	DE Morgan's Theorem
Week 8	Karnaugh Map
Week 9	Combinational Logic Circuit
Week 10	Functions of Combinational Logic
Week 11	Latches
Week 12	Flip-Flops
Week 13	Counters
Week 14	Counters
Week 15	Multiplexer and demultiplexer

Delivery Plan (Weekly Lab. Syllabus)
المنهاج الاسبوعي للمختبر

	Material Covered
Week 1	Introduction to Digital Logic and Logic Gates
Week 2	Logic Gates and Truth Tables
Week 3	Logic Gate Implementations
Week 4	Combinational Logic Circuits
Week 5	Multiplexers and Demultiplexers
Week 6	Encoders and Decoders
Week 7	Sequential Logic Circuits: Latches and Flip-Flops
Week 8	Sequential Logic Circuits: Counters
Week 9	Shift Registers
Week 10	Memory Units: RAM and ROM
Week 11	Introduction to Programmable Logic Devices
Week 12	Number Systems: Binary, Decimal, and Hexadecimal
Week 13	Number System Conversions
Week 14	Arithmetic Circuits: Adders and Subtractors
Week 15	Digital Logic Design Project

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Digital Logic & Number System (Munich war Gulati & Mini) Gulati)	
Recommended Texts	Digital logic and computer design (Morris-Mano) 4th ed.	
Websites		

Grading Scheme مخطط الدرجات				
Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.